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09/975,202	10/11/2001	Koji Ishii	AUS920010940US1	8813

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EXAMINER	
VU, TRISHA U	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/975,202	ISHII, KOJI	
	Examiner	Art Unit	
	Trisha U. Vu	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 18 recites the limitation "said second switch means" in lines 4-5. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 4, 7, 12, 13, 15, 16, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Evoy (6,044,412).

As to claim 1, Evoy teaches an interface circuit for interfacing a system controller integrated circuit and a plurality of peripheral integrated circuits (Fig. 1), said interface circuit comprising: a node (pin 105, 107, and/or 109) within said system controller

integrated circuit commonly connected to a first and a second one of said plurality of peripheral integrated circuits (IDE110, ROM 120, MODEM 130); first switch means (MUX 201) for selectively connecting said node to a first circuit of the systems controller integrated circuit for communicating signals with reference to said first peripheral integrated circuit; second switch means (MUX 201) for selectively connecting said node to a second circuit of the systems controller integrated circuit for communicating signals with reference to said second peripheral integrated circuit (col. 3 line 1 to col. 4 line 9) ; signal means (ARB 203) for early enabling and late disabling of said first and second switch means consistent with setup and hold times of the respective first and second peripheral integrated circuits (Fig. 2, and col. 4, lines 1-20 wherein the early enabling and late disabling are inherent in the system since selection and disabling must be made beforehand and afterward respectively; also, arbitration logic 201 ensures that conflict between the devices in relation to the shared pins is avoided (col. 4, lines 11-20)).

As to claim 2, Evoy further teaches the node is an output pin for providing an output signal to said first one and said second one of said plurality of peripheral integrated circuits (e.g. pin 107 performs ROM address output, IDE data output) (col. 3, lines 1-12), and wherein said first switch means comprises a selector (MUX 201) within said system controller integrated circuit having a select input coupled to signal means (Fig. 2 and col. 3 line 63 to col. 4, line 9).

As to claim 4, Evoy further teaches said first circuit is a data signal generator and said second circuit is an address generator (e.g. generating D[15-0] and A[20:0]) (Figs. 1-2).

As to claim 7, Evoy further teaches said node is an input pin for receiving a first signal from said first peripheral integrated circuit and a second signal from said second peripheral integrated circuit (Fig. 2).

As to claim 12, Evoy teaches method for coupling a plurality of signals of differing types between a plurality of peripheral integrated circuits (110, 120, 130) and a system controller integrated circuit (system controller) (Fig. 1), said method comprising: generating a peripheral select signal within said system controller integrated circuit for early enabling and late disabling switch means consistent with setup and hold times of the peripheral integrated circuits (by ARB 203) (Fig. 2, and col. 4, lines 1-20 wherein the early enabling and late disabling are inherent in the system since selection and disabling must be made beforehand and afterward respectively; also, arbitration logic 201 ensures that conflict between the devices in relation to the shared pins is avoided (col. 4, lines 11-20)).; generating a chip select signal from said peripheral select signal; supplying said chip select signal to a corresponding peripheral integrated circuit chip select input (e.g. ROMCS#); selecting one of a plurality of internal signals each associated with one of said plurality of peripheral integrated circuits in conformity with said peripheral select signal; and coupling said selected internal signal to an external pin connected to each of said plurality of peripheral integrated circuits (Fig. 2), whereby said selecting and said coupling interface a internal signal associated with a peripheral integrated circuit corresponding to said chip select signal (Fig. 2 and col. 3 line 1 to col. 4 line 9).

As to claim 13, Evoy further teaches said selecting selects one of said plurality of internal signals at a time preceding said generating by a time greater than or equal to a maximum setup time among said first and second peripheral integrated circuits and continues to select said selected one of said plurality of internal signals until said generating is complete and a time greater than or equal to a maximum hold time among said first and second peripheral integrated circuits has elapsed (col. 4, lines 11-20).

As to claim 15, Evoy further teaches latching a signal value received from said external pin resulting from said coupling at an end said generating; and holding said signal value to maintain a state of one of said plurality of internal signals after an end of said coupling (Fig. 2 and col. 4, lines 11-20).

As to claim 16, Evoy teaches an interface circuit for interfacing a system controller integrated circuit and a plurality peripheral integrated circuits (Fig. 1), said interface circuit comprising: a node (pin 105, 107, and/or 109) within said system controller integrated circuit commonly connected to a first and a second one of said plurality of peripheral integrated circuits; a selector (MUX 201) for selectively connecting said node to one of a first circuit of the systems controller integrated circuit for communicating signals with reference to said first peripheral integrated circuit and a second circuit of the systems controller integrated circuit for communicating signals with reference to said second peripheral integrated circuit; a chip select circuit (by ARB 203 and associate circuitry) providing a first chip select output for connection to a first chip select input of said first peripheral integrated circuit and a second chip select output for connection to a second chip select input of said second peripheral integrated circuit and

an selection signal connected to said selector, wherein said selection signal is set to a state for selecting one of said first circuit and said second circuit at a time preceding assertion one of said chip select signals by a time greater than or equal maximum setup time among said first and second peripheral integrated circuits and is maintained in that state until said asserted one of said chip select signals is de-asserted and a time greater than or equal to a maximum hold time among said first and second peripheral integrated circuits has elapsed (Fig. 2, and col. 4, lines 1-20 wherein it is inherent in the system that selection and disabling must be made beforehand and afterward respectively; also, with respect to setup and hold time, arbitration logic 201 ensures that conflict between the devices in relation to the shared pins is avoided (col. 4, lines 11-20)).

As to claim 18, Evoy further teaches said node (pin 105, 107, and/or 109) is a pin for receiving a first signal from said first peripheral integrated circuit and transmitting a second signal to said second peripheral integrated circuit (Fig. 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy (6,044,412) in view of Chan et al. (Pub. No. 2002/0052990) (hereinafter Chan).

As to claim 3, the argument above for claim 2 applies. Evoy further teaches said first peripheral integrated circuit is a memory device (ROM 120) (Fig. 1), said second peripheral integrated circuit is an IDE device (IDE 110) (Fig. 1), said first circuit is an address generator (for generating address A[20:5]) and said second circuit is a bus control generator (e.g. generating IDE_IOR#, IDE_IOW#) (Figs. 2-3). However, Evoy does not explicitly disclose the second peripheral integrated circuit is a bus controller. Chan teaches IDE bus controller (Fig. 7 and paragraph [0081]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement IDE bus controller as the second peripheral integrated circuit in the system of Evoy as taught by Chan to provide the system with additional functions/capabilities such as CD drive, CD drive, or other IDE media device (paragraph [0081]).

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy (6,044,412) in view of Clark et al. (Pub. No. 2002/0005225) (hereinafter Clark).

As to claim 5, the argument above for claim 2 applies. However, Evoy does not explicitly disclose selectively connecting the first circuit and second circuit using a tri-state buffer having an input coupled to said first circuit, an output coupled to said node, and an enable input coupled to said signal means; and a second tri-state buffer having an input coupled to said second circuit, an output coupled to said mode, and an disable input coupled to said signal means. Clark teaches selectively connecting a first circuit (by 72) and a second circuit (by 74) using a first tri-state having an input coupled to the first circuit, an output coupled to a node (42), and an enable input coupled to a signal means

(CLK); and a second tri-state buffer having an input coupled to said second circuit, an output coupled to said node, and an disable input coupled to said signal means (Fig. 2 and paragraph [0032]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the two tri-state buffers to selectively connecting circuits as taught by Clark in place of the multiplexer in the system of Evoy to provide each connection the flexibility to be switched reversibly, also tri-state buffer minimizes current leakage.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy (6,044,412) in view of Houg (6,324,596).

As to claim 6, the argument above for claim 2 applies. Evoy further teaches the first and said second switch means comprise: a multiplexer (201) having inputs coupled to said first circuit and said second circuit and a select input coupled to said signal means. However, Evoy does not explicitly disclose an output coupled between said multiplexer and said node. Houg teaches output driver (412) (Fig. 4 and col. 4, lines 50-53). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include an output driver as taught by Houg in the system of Evoy to transmit signals from the multiplexer.

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7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy (6,044,412) in view of Clark et al. (Pub. No. 2002/0005225) (hereinafter Clark) and further in view of Richard (4,756,006).

As to claim 8, the argument above for claim 7 applies. Evoy further teaches first chip select signal means (e.g. IDE_CS0#) coupled to said first peripheral integrated circuit for enabling communication with said first peripheral integrated circuit; second chip select signal means (ROMCS#) coupled to said second peripheral integrated circuit for enabling communication with said second peripheral integrated circuit. However, Evoy does not explicitly disclose selectively connecting the first circuit and second circuit using a first transparent latch having a gate input coupled to said first chip select signal means, whereby a state of said node may be maintained at said first circuit when said signals means deselects communication said first peripheral integrated circuit, and a second transparent latch having a gate input coupled to said second chip select signal means, whereby a state of said node may be maintained at said second circuit when said signal means deselects said second peripheral integrated circuit. Clark teaches selectively connecting a first circuit (by 72) and a second circuit (by 74) using a first tri-state having an input coupled to the first circuit, an output coupled to a node (42), and an enable input coupled to a signal means (CLK); and a second tri-state buffer having an input coupled to said second circuit, an output coupled to said node, and an disable input coupled to said signal means (Fig. 2 and paragraph [0032]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the two tri-state buffers to selectively connecting circuits as taught by Clark in place of the multiplexer in the system of Evoy to provide each connection the flexibility to be switched reversibly, also tri-state buffer minimizes current leakage. However, Evoy and Clark do not explicitly disclose implementing a first latch and a second latch in place of a first tri-state

buffer and a second tristate buffer. Rickard teaches a latch (e.g. 26) (Fig. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement latch as taught by Rickard in place of tristate buffer in the system of Evoy and Clark because latch can be manufactured easily at a relatively low cost.

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy (6,044,412) in view of Gradinariu (6,378,008).

As to claim 9, the argument above for claim 1 applies. Evoy further teaches said node is a pin for receiving a first signal from said first peripheral integrated circuit and transmitting a second signal to said second peripheral integrated circuit (Fig. 2). However, Evoy does not explicitly disclose said second switch means comprises a tri-state buffer having an enable input coupled to said signal means an output coupled to said node and an input coupled to said first circuit. Gradinariu teaches tristate buffers (410, 420) (Fig. 4) for receiving input signal and transmitting output signal. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement input tristate buffer and output tristate buffer as taught by Gradinariu in the system of Evoy to provide each connection the flexibility to be switched reversibly, also tri-state buffer minimizes current leakage.

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9. Claims 10 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy (6,044,412) in view of Gradinariu (6,378,008) and further in view of Richard (4,756,006).

As to claim 10, the argument above for claim 9 applies. However, Evoy and Gradinariu do not explicitly disclose a transparent latch in place of the tristate buffer. Rickard teaches a transparent latch (e.g. 26) (Fig. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement transparent latch as taught by Rickard in place of tristate buffer in the system of Evoy and Gradinariu because latch can be manufactured easily at a relatively low cost.

As to claim 17, the argument above for claim 16 applies. However, Evoy does not explicitly disclose a transparent latch having an input coupled to an output of said selector, whereby a state of said node that reflects an output of said selected one of said peripheral integrated circuits is held after said asserted one of said chip select signals is de-asserted. Gradinariu teaches tristate buffers (410, 420) (Fig. 4) for receiving input signal and transmitting output signal. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement input tristate buffer and output tristate buffer as taught by Gradinariu in the system of Evoy to provide each connection the flexibility to be switched reversibly, also tri-state buffer minimizes current leakage. However, Evoy and Gradinariu do not explicitly disclose a transparent latch in place of the tristate buffer. Rickard teaches a transparent latch (e.g. 26) (Fig. 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement transparent latch as taught by Rickard in place of tristate buffer in the system of Evoy and Gradinariu because latch can be manufactured easily at a relatively low cost. (With respect to setup and hold time, arbitration logic 201 of Evoy ensures that conflict between the devices in relation to the shared pins is avoided (col. 4, lines 11-20)).

10. Claims 11, 14, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy (6,044,412) in view of Clark et al. (Pub. No. 2002/0005225) (hereinafter Clark) and further in view of Kudou (5,363,494).

As to claims 11 and 14, the argument above for claims 1 and 12 apply. However, Evoy does not explicitly disclose said node is a bi-directional interface pin for interfacing bidirectional signals to said first and said second peripheral integrated circuits, wherein said first circuit and said second circuit include bidirectional input/output connections, wherein said first switch means comprises a transmission gate having a select input coupled to said signal means, a first terminal connected to said node and a second terminal coupled to said first circuit, and wherein said second switch means comprises a transmission gate having a select input coupled to said signal means, a first terminal connected to said node and a second terminal coupled to said second circuit. Clark teaches selectively connecting a first circuit (by 72) and a second circuit (by 74) using a first tri-state having an input coupled to the first circuit, an output coupled to a node (42), and an enable input coupled to a signal means (CLK); and a second tri-state buffer having an input coupled to said second circuit, an output coupled to said node, and an disable input coupled to said signal means (Fig. 2 and paragraph [0032]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the two tri-state buffers to selectively connecting circuits as taught by Clark in place of the multiplexer in the system of Evoy to provide each connection the flexibility to be switched reversibly, also tri-state buffer minimizes current leakage. However, Evoy

and Clark do not explicitly disclose the node is bi-directional interface pin for interfacing bidirectional signals to first and second circuits, said first circuit and said second circuit include bidirectional input/output connections. Kudou teaches bi-directional input/output connections (bi-directional buffer 16a constituted by a plurality of bit lines having a pair of tri-state buffer circuits 34-1 and 34-2) (Fig. 5 and col. 4, lines 14-35). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement bidirectional input/output connection as taught by Kudou in place of tri-state buffer in the system of Evoy and Clark to provide signal transmission in both directions.

As to claims 19-20, the argument above for claim 1. However, Evoy does not explicitly disclose said node is a bi-directional interface pin for interfacing bidirectional signal to said first and said second peripheral integrated circuits, wherein said first circuit and said second circuit include bidirectional input/output connection, and wherein said selector comprises a transmission gate having a select input coupled to said chip select circuit, a first terminal connected to said node and a second terminal coupled to said first circuit, and wherein said selector further comprises a second transmission gate having a select input coupled to said chip select circuit, a first terminal connected to said node and a second terminal coupled to a bi-directional signal of said second circuit. Clark teaches selectively connecting a first circuit (by 72) and a second circuit (by 74) using a first tri-state having an input coupled to the first circuit, an output coupled to a node (42), and an enable input coupled to a signal means (CLK); and a second tri-state buffer having an input coupled to said second circuit, an output coupled to said node, and an disable input coupled to said signal means (Fig. 2 and paragraph [0032]). It would have been obvious

to one of ordinary skill in the art at the time the invention was made to implement the two tri-state buffers to selectively connecting circuits as taught by Clark in place of the multiplexer in the system of Evoy to provide each connection the flexibility to be switched reversibly, also tri-state buffer minimizes current leakage. However, Evoy and Clark do not explicitly disclose the node is bi-directional interface pin for interfacing bidirectional signals to first and second circuits, said first circuit and said second circuit include bidirectional input/output connections. Kudou teaches bi-directional input/output connections (bi-directional buffer 16a constituted by a plurality of bit lines having a pair of tri-state buffer circuits 34-1 and 34-2) (Fig. 5 and col. 4, lines 14-35). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement bidirectional input/output connection as taught by Kudou in place of tri-state buffer in the system of Evoy and Clark to provide signal transmission in both directions.

Response to Arguments

11. Applicant's arguments filed 07-19-04 have been fully considered but they are not persuasive:

With respect to Applicant's argument on page 12 that "Evoy does not teach that early enabling and late disabling consistent with the setup and hold times of the devices is performed", it is noted that "early enabling" and "late disabling" are taught in Evoy since selection and disabling must be made beforehand and afterward respectively. Aslo, as indicated in the interview with Applicant's representative on 07-12-04, the Examiner had pointed out that

Applicant has not addressed in the claims how "late disabling" and "early enabling" are different from Evoy.

With respect to Applicant's argument on page 4 of the Remarks that "in Kudou, the bi-directional buffer is enabled for one direction of data flow at a time, and therefore would does not provide the functionality of a transmission gate", it is noted that Evoy and Clark already taught transmission gate, Kudou was brought in to show bi-directional communication which is applied to the tristate-buffer(s) of Clark. Applicant further stated that "Grandinaru teaches a pair of tri-state buffers, the output buffer is coupled to another bus line, not the same bus line as in the present invention", note Fig. 2 of Grandinaru where the output of the tri-state buffers is coupled to same bus line (44).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha U. Vu whose telephone number is 703-305-5959. The examiner can normally be reached on Mon-Thur and alternate Fri from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trisha Vu

Trisha U. Vu
Examiner
Art Unit 2112

uv

Sumati Lefkowitz

SUMATI LEFKOWITZ
PRIMARY EXAMINER